REMARKS

Prior to the present amendment and response, claims 1-9, 11-15, and 21-28 were pending in the present application. By the present amendment and response, claims 1-9, 11-15, and 21-28 have been canceled and claims 29-46 have been added. Thus, claims 29-46 remain in the present application. In view of the following remarks, allowance of outstanding claims 29-46 is respectfully requested.

A. Patentability of Claims 29-46 over Cited Art

The Examiner has rejected claims 1-9 and 11-28 under 35 USC §102(e) as being anticipated by U.S. Patent Number 6,615,338 to Tremblay, et al. (hereinafter "Tremblay"). By the present amendment and response, Applicants have canceled claims 1-9, 11-15, and 21-28 and have added claims 29-46. For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 29, 34, and 40, is patentably distinguishable over Tremblay.

The present invention, as defined by independent claim 29, recites, among other things, first and second instruction packets each comprising at most two issue groups, where each of the at most two issue groups of each of the first and second instruction packets comprise at most 64 bits and require an internal instruction bus no greater than 64 bits wide for transport to one of first and second processing units in respective first and second threads. As disclosed in the present application, the present invention is directed to a two-thread processor, where each thread is required to process an issue group (e.g.,

issue groups 422 and 424 in VLIW packet 410 and issue groups 442 and 444 in VLIW packet 430) having at most 64 bits. Additionally, in one embodiment of the present invention, an instruction packet (e.g., VLIW packet 410 in Figure 4A and VLIW packet 430 in Figure 4B) comprises at most two issue groups.

By limiting each instruction packet to at most two issue groups and limiting each issue group to at most 64 bits, the present invention, as defined by independent claim 29, advantageously reduces the unnecessary power consumption resulting from conventional approaches. One reason for such unnecessary power consumption in conventional VLIW processors is illustrated with the aid of an example provided by reference to Figure 2 of the present application:

> "After exemplary VLIW packet 200 is fetched from a cache or an external memory, the four instructions in VLIW packet 200 must be forwarded to appropriate execution units for execution. To account for the possibility that all of the instructions in a given VLIW packet may belong to a single issue group, the instruction bus coupled to the execution units of the VLIW processor must be 112 bits wide to carry all four instructions in the VLIW packet at the same time. However, as illustrated in the present example, the first issue group consists of merely two long instructions requiring an instruction bus that is only 64 bits wide while the second issue group consists of merely one long instruction and one short instruction requiring an instruction bus that is only 48 bits wide. Thus, in the case of exemplary VLIW packet 200, an instruction bus that is 64 bits wide is all that is needed to handle the processing of both the first and second issue groups in the VLIW packet. As such, a 112-bit wide instruction bus would result in an unnecessary power consumption associated with 48 bus lines that are not needed in the processing of exemplary VLIW packet 200. Further, an instruction bus which is 112 bits wide requires considerably greater chip area as compared with an instruction bus which is only 64 bits wide." Page 4, line 20 to page 5, line 12 of the present application.

Thus, conventional VLIW processors have an architectural limitation which not only results in excess power consumption, but also require a relatively large chip area and extra power for instruction buses that are wider than necessary. In contrast, the present invention, as defined by independent claim 29, specifically requires a busing architecture with internal buses (e.g., internal instruction buses 370 and 380 in Figure 3) no greater than 64 bits wide for transport of issue groups to each thread of the VLIW processor.

In contrast to the present invention as defined by independent claim 29, Tremblay does not teach, disclose, or suggest first and second instruction packets each comprising at most two issue groups, where each of the at most two issue groups of each of the first and second instruction packets comprise at most 64 bits and require an internal instruction bus no greater than 64 bits wide for transport to one of first and second processing units in respective first and second threads. Tremblay is directed to a VLIW processor containing independent clustered functional units capable of parallel processing of instructions. Tremblay specifically discloses core processor 100 including media processing units 110, where media processing units 110 each include instruction cache 210, instruction aligner 212, instruction buffer 214, pipeline control unit 226, split register file 216, execution units, which include three media functional units (MFU) 220 and one general functional unit (GFU) 222, and load/store unit 218. *See*, e.g., column 6, lines 51-67 and Figure 3 of Tremblay.

However, Tremblay fails to teach, disclose, or remotely suggest first and second instruction packets each comprising at most two issue groups, where each of the at most

two issue groups of each of the first and second instruction packets comprise at most 64 bits and require an internal instruction bus no greater than 64 bits wide for transport to one of first and second processing units in respective first and second threads, as specified by independent claim 29. In contrast, Tremblay discloses multiple operations packaged into one very long instruction, where the multiple operations are determined by subinstructions that are applied to independent functional units. *See*, e.g., Tremblay, column 1, lines 64-67. In Tremblay, typical bit lengths of a subinstruction commonly range from 16 to 64 bits per functional unit to produce an instruction length often in a range from 64 to 512 bits for VLIW groups from four to eight subinstructions. *See*, e.g., Tremblay, column 1, line 67 to column 2, lines 1-5. However, Tremblay fails to even mention issue groups.

On page 9 of the Office Action dated December 29, 2005, the Examiner states that "[in] Tremblay, the VLIW groups, not to be confused with issue groups, are the packets and the subinstructions, are the issue groups." However, Tremblay discloses that highly parallel computing applications that have few data dependencies and few branches are executed most efficiently using a wide VLIW processor with a greater number of subinstructions in a VLIW group. *See*, e.g., Tremblay, column 2, lines 60-64. Thus, Applicants respectfully submit that "subinstructions" in Tremblay refer to individual instructions, such as "shift," "add," or "subtract" instructions. As such, an issue group, which is not disclosed in Tremblay, would include a group of subinstructions that could be executed in one clock cycle. Thus, Applicants respectfully submit that the

subinstructions disclosed in Tremblay are similar to individual instructions disclosed in the present application, such as instructions 414, 416, 418, or 420 in VLIW packet 410 in Figure 4A. Thus, Tremblay fails to teach, disclose, or remotely suggest limiting an instruction packet in a VLIW processor to at most two issue groups and limiting each issue group in the instruction packet to at most 64 bits, as specified in independent claim 29.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by independent claim 29, is not taught, disclosed, or suggested by Tremblay. Thus, independent claim 29 is patentably distinguishable over Tremblay and, as such, claims 30-33 depending from independent claim 29 are, *a fortiori*, also patentably distinguishable over Tremblay for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Independent claims 34 and 40 include similar limitations as independent claim 29. Thus, for similar reasons as discussed above, independent claims 34 and 40 are also patentably distinguishable over Tremblay. As such, claims 35-39 depending from independent claim 34 and claims 41-46 depending from independent claim 40 are, *a fortiori*, also patentably distinguishable over Tremblay for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 29, 34, and 40 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 29-46 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 29-46 pending in the present application is respectfully requested.

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Respectfully Submitted,
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